Current HPC ecosystems rely upon Commercial Off-the-Shelf (COTS) building blocks to enable cost-effective design by sharing costs across a larger ecosystem. Modern HPC nodes use commodity chipsets and processor chips integrated together on custom motherboards. Commodity HPC is heading into a new era where the chip acts as the "silicon motherboard" that interconnects commodity Intellectual Property (IP) circuit building blocks to create a complete integrated System-on-a-Chip (SoC). These SoC designs have the potential for higher performance at better power efficiency than current COTS solutions. Going further, a custom SoC could potentially contain a diverse collection of accelerators that could enhance performance and reliability at all levels of the software stack—from applications to runtimes. To properly explore this broad design space, DE/HPC is focusing on the development of the tools to enable the creation of custom SoC architectures tailored to the needs of HPC. The large-scale emulation environment shown here will demonstrate how we are building the tools needed to evaluate new and novel architectures at speeds fast enough to evaluate whole application performance.

**IP Shopping List: What do we need to build a semi-custom SoC?**

An alternative model for commodity HPC is emerging where the chip acts as the "silicon motherboard" that interconnects commodity Intellectual Property (IP) circuit building blocks to create a complete integrated SoC—a common practice in the fast growing and innovative embedded processing market. By leveraging the enormous commodity IP market for design tools, processors, memory controllers, and I/O circuit designs, a chip designer can focus their effort and NRE costs on engineering a handful of essential features that are not covered by the commodity ecosystem allowing the rapid creation of semi-custom designs. This presents a new design paradigm and architecture for HPC, cloud, and high performance embedded systems.

**Emergence of Open Source IP**

In lieu of relying exclusively on commercial IP, we are focused on bringing together multiple, emerging open source technologies in novel ways to create new tools and techniques to enable advanced architectural exploration.

**A Large Scale SoC Exploration Platform**

The FPGA system is a collection of PCIe backplanes, each with six FPGA modules. The FPGAs are able to communicate over a PCIe Switch on each of the FPGA PCIe backplanes. Each backplane can communicate with others through the PCIe root complex on the server’s motherboard. Inside each FPGA, the FPGAs can communicate using OpenSoC Fabric with the network ports divided between Z-scale RISC-V cores, the FPGAs module’s 8GB DRAM and the off-chip network between the FPGA backplanes. The large scale emulation system demonstrated provides a realistic proving ground for advanced hardware architectures, programming models, runtime and applications research by providing an early test-bed for experimentation.